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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,325	12/03/2001	Kunihiko Tani	XA-9589	5539

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EXAMINER	
DEWITTE, CONRAD J	

ART UNIT	PAPER NUMBER
2673	3

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,325	TANI ET AL.	
	Examiner	Art Unit	
	Conrad J. DeWitte	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11, and 13-24* is/are rejected.

7)☒ Claim(s) *10-13, 18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to because:

- Fig. 11: Memory Array (Display RAM) not labeled 140 as indicated in Specification p. 2, line 9.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because

- They include the following reference sign not mentioned in the description: element 180 in Figure 2
- They do not include the following reference sign mentioned in the Specification at page 19, line 12: element 170

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

It is not clear by Figures 2, 3, and 4 how the memory array 141 shown in Figures 3 and 4 is connected to the liquid crystal control driver 100 shown in Figure 2. Applicant should amend the drawings to indicate how the memory array 141 is connected to the liquid crystal control driver 100.

Specification

5. The abstract of the disclosure is objected to because:

- Applicant used "th" not "the" in line 3. Correction is required. See MPEP § 608.01(b)
- The abstract exceeds 150 words (see 37 CFR 1.72(b))

6. The disclosure is objected to because of the following informalities:

- Applicant used "or" not "of" at page 2, line 15.
- Applicant should include a definition of the term "LSI" found on page 3, line 7.
- Applicant used "th" not "the" at page 3, line12.
- The paragraph beginning at page 3, line 23, and ending on page 4, line 25 is one sentence comprised of claim 1. Likewise, the paragraph beginning on page 5, line 1, and the paragraph beginning on page 5, line 19 similarly include run on sentences which are apparently versions of one or more of the claims This is certainly not in the spirit of MPEP § 608.01(d), and 37 CFR 1.73. Examiner

requests Applicant to revise these paragraphs so that they may properly "apprise the public . . . of the nature of the invention." MPEP § 608.01(d).

- At page 6, lines 21-22, it is unclear what Applicant means by "the number of the first data latch means is an integral multiple further of the n times." Examiner requests Applicant to revise this sentence.
- Applicant used "of" not "on" at page 9, line11.
- It is unclear to what the applicant is referring by "(e.g. 384)" and "(e.g. 176)" at page 13, lines 6 and 8, respectively.
- Applicant used "of" not "with" at page 14, line 7.
- Applicant used "BL15 /BL15" not "BL15, /BL15" at page 20, line 4.
- Applicant used "blank box" not "filled-in box" at page 30, line 16.

Appropriate correction is required.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8. Claim 10 is objected to because of the following informality:

Claim 10 appears to be dependent on claim 9, not claim 15, both because of the language of claim 10, and because a claim should depend on a preceding claim not on a later claim. The Examiner has reviewed this claim assuming that it in fact is dependent on claim 9, not claim 15.

9. Claim 11 is objected to because of the following informality:

Page 38, line 9: Used "(multiple by n)" not "(multiple of n)" or "(multiplied by n)"

10. Claim 12 is objected to because of the following informality:

Page 38, lines 17-18: Used "said number of bits (k•n)" not "said m bits (k•n)."

11. Claim 13 is objected to because of the following informality:

Page 39, line 5: Used "(multiple by n)" not "(multiple of n)" or "(multiplied by n)"

12. Claim 18 is objected to because of the following informality:

Page 40, line 19: Used "(multiple by n)" not "(multiple of n)" or "(multiplied by n)"

13. Claim 21 is objected to because of the following informality:

Page 42, line 12: Used "(multiple by n)" not "(multiple of n)" or "(multiplied by n)"

14. Appropriate correction is required.

Claim Rejections - 35 USC § 112

15. Claims 3 through 9 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Claim 3 recites the limitations "the same timing as the final data" at lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 4 recites the limitation "the number of said first data latch means" at line 2. There is insufficient antecedent basis for this limitation in the claim.

18. Claim 6 recites the limitations "the start address" at line 2; "the quantity of data" at lines 3-4; and "the end address" at line 4. There is insufficient antecedent basis for these limitations in the claim.

19. Claim 8 recites the limitation "their writing position" at line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. Claim 1 is rejected under 35 U.S.C. 102(b) as being unpatentable over the combination of Taylor (U.S. Pat. No. 5,844,856), and Rao (U.S. Pat. No. 5,687,132) (because Taylor incorporates by reference Rao as a source of supplemental information in the disclosure; *see* Taylor, col. 5, lines 48-52).

22. Taylor discloses a display control device (col. 3, lines 3-4) comprising a display memory (col. 2, line 65 to col. 3, line 7), the display control device successively reading the display data out of the display memory and forming and supplying a drive signal to the display device (col. 3, lines 3-4), wherein said display memory includes a memory array provided with a plurality of memory cells arranged in a matrix form (col. 4, lines 36-63; Fig. 1, elements 100, 102), a plurality of word lines to which selection terminals for the memory cells are connected (col. 4, lines 64-65; Fig. 2, element 104), a plurality of bit lines which are arranged in a direction to cross the word lines and to which data input/output nodes for the memory cells are connected (col. 5, lines 3-16; Fig. 2, element 110, 112), and input transfer means (col. 5, lines 8-16; Fig. 2, elements 114, 116) and output transfer means (col. 5, lines 26-29) being connected to said bit lines (Fig. 2, elements 110, 112, 114, 116).

23. Taylor does not itself disclose a display memory that is capable of storing display data for a display device and "into which display data are written in a prescribed number of bits at a

time." Furthermore, Taylor does not itself disclose "data transferring by said input transfer means resulting in writing of data into the memory cells connected to a word line in a selected state, and data transferring by said output transfer means resulting in reading of data out of the memory cells connected to the word line in a selected state, and wherein said display memory further includes a plurality of first data latch means capable of successively taking in the display data in said prescribed number of bits at a time."

24. Rao (which was incorporated by reference by Taylor) discloses a display memory, which is capable of storing display data for a display device and into which display data are written in a prescribed number of bits at a time, (col. 3, lines 1-14). Rao also discloses data transferring by said input transfer means resulting in writing of data into the memory cells connected to a word line in a selected state, (col. 9, lines 36-67; Fig. 3, elements 201, 202), and data transferring by said output transfer means resulting in reading of data out of the memory cells connected to the word line in a selected state, (*id.*), and wherein said display memory further includes a plurality of first data latch means capable of successively taking in the display data in said prescribed number of bits at a time, (col. 9, lines 6-13; Fig. 3, element 208).

25. Rao does not disclose the display data held by the first data latch means can be collectively transferred by said input transfer means to the bit lines of said display memory in a number of bits at a time equal to an integral multiple of (n times) the number of bits of the display data taken into the first data latch means. However, Taylor discloses this feature at col. 8, lines 50-55.

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor and Rao as applied to claim 1 above, and further in view of Nitta et al. (U.S. Pat. No. 6,448,976).

28. Regarding claim 2, Taylor and Rao fail to disclose a plurality of second data latch means capable of taking in display data held by said first data latch means in a number of bits at a time equal to an integral multiple of the number of bits of the display data taken into said first data latch means.

Nitta et al. discloses a plurality of second data latch means capable of taking in display data held by said first data latch means in a number of bits at a time equal to an integral multiple of the number of bits of the display data taken into said first data latch means. Col. 5, lines 40-63; Fig. 1, elements 103, 104.

Taylor discloses the input transfer means are configured to be capable of transferring display data held by the second data latch means to the bit lines of said display memory in a number of bits at a time equal to an integral multiple of (n-times) the number of bits of the display data taken into said first data latch means. Col. 8, lines 50-55.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to further combine the teachings of Taylor and Rao with Nitta et al. because Nitta et al. discloses a liquid crystal drive circuit, Taylor discloses a dual port memory, and it is

conventional in the art that a liquid crystal driver circuits contain a memory to hold and control the data to display.

29. Regarding claim 3, Taylor discloses transferring of data by said input transfer means to the bit lines of said display memory takes place at the same timing as the final data taken into said first data latch means. Col. 8, lines 59-65.

30. Regarding claim 4, Rao discloses the number of said first data latch means is an integral multiple further of said n times. Col. 9, lines 48-50.

31. Regarding claim 5, Taylor discloses a mask setting means capable of setting the number of bits of data to be transferred by said input transfer means to the bit lines of said display memory, wherein said input transfer means is controlled on the basis of the set information of the mask setting means. Col. 5, lines 30-52; Fig. 1.

32. Regarding claim 6, Taylor discloses that the mask setting means can set the start address of write data in a range of consecutive addresses and the quantity of data to be masked from that start address and the end address of the same and the quantity of data to be masked from that end address. Col. 5, lines 30-52.

33. Regarding claim 7, Nitta et al. discloses segment drive means for generating signals for driving segment electrodes of an external liquid crystal display device on the basis of display data read out of said display memory, wherein said display control device is configured as a semiconductor integrated circuit over a single semiconductor chip. Col. 10, lines 8-26; Fig. 8, element 801.

34. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor and Rao as applied to claim 1 above, and further in view of Yamazaki et al. (U.S. Pat. No. 6,147,667), and Furuhashi et al. (U.S. Pat. No. 6,384,807 B1).

35. Regarding claim 8, Taylor and Rao fail to disclose a mobile electronic apparatus with a display comprising a data processing unit for generating display data to be written into said display memory and setting information on their writing position, and a display device for carrying out displaying with a display drive signal read out of said display memory and formed by said display control device on the basis of the display data.

Yamazaki et al. discloses a mobile electronic apparatus with a display. Col. 30, line 30 to col. 31, line 10; Fig. 19A-E. However, Yamazaki does not disclose a data processing unit for generating display data to be written into said display memory and setting information on their writing position, and a display device for carrying out displaying with a display drive signal read out of said display memory and formed by said display control device on the basis of the display data.

Furuhashi et al. discloses a data processing unit for generating display data to be written into said display memory and setting information on their writing position, and a display device for carrying out displaying with a display drive signal read out of said display memory and formed by said display control device on the basis of the display data. Col. 43, lines 39-50; Fig. 23, Fig. 5.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Taylor and Rao with Yamazaki because the combination of the control device of claim 1 and the electronic apparatus disclosed in Yamazaki is conventional, and the use

of Taylor and Rao with Yamazaki would allow for the display to be controlled more efficiently. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Taylor and Rao with Furuhashi et al. because Furuhashi et al discloses a liquid crystal display driving circuit, which is analogous to the art disclosed in Rao. Furthermore, Taylor discloses a dual port memory, and it is conventional in the art that many liquid crystal driver circuits contain a memory. Additionally, Yamazaki is also directed to a display device.

36. Regarding claim 9, Furuhashi et al. further discloses that the display device is a dot matrix type liquid crystal display device. Figs. 5, 23.

37. Claims 11-16, and 18, 19, and 21, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo et al. (U.S. Pat. No. 6,353,435 B2) in further in view of Nakano et al. (U.S. Pat. No. 6,529,181 B1).

38. Regarding claim 11, Kudo et al. discloses a memory for storing display data to be displayed on a liquid crystal panel (col. 13, line 26 to col. 15, line 23), a k-bit first external terminal to which display data to be stored in said memory are supplied from a microprocessor (col. 9, lines 7-30; Fig. 2, element 21), a first latch circuit connected between the input of said memory and said first external terminal and capable of storing m-bit display data (col. 12, lines 19-24); and a transfer circuit for selecting, for each integral multiple (multiple by n) of said k bits, display data of not more than said m bits (k•n) in said first latch circuit and transferring them to bit lines of said memory (col. 12, line 30 to col. 13, line 47; Fig. 2, element 24). However, Kudo et al. does not disclose a display control device formed over a single

semiconductor substrate, comprising a plurality of second external terminals for outputting drive signals for driving said liquid crystal panel on the basis of m-bit read data from said memory.

39. Nakano et al. discloses a display control device formed over a single semiconductor substrate (col. 6, lines 22-23), comprising a plurality of second external terminals for outputting drive signals for driving said liquid crystal panel on the basis of m-bit read data from said memory (col. 6, lines 6-11; Fig. 1, element 21).

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakano et al. and Kudo et al. because both Nakano and Kudo disclose liquid crystal display apparatuses, and their combination leads to a more desirable and efficient liquid crystal display control apparatus.

41. Regarding claim 13, Kudo et al. further discloses that said display control device has a control register for setting a first operating mode and a second operating mode (col. 13, lines 50-58; Fig. 1, elements 25, 26); the mode of writing into said memory is set in said first operating mode in response to the setting of a first value into said control register, wherein the mode of writing into said memory is set in said second operating mode in response to the setting of a second value into said control register (col. 13, lines 54-60; Fig. 5); and said transfer circuit transfers, for each integral multiple (multiple by n) of said k bits stored in said first latch circuit, said display data to bit lines of said memory in response to setting into said first operating mode (col. 13, lines 54-57; Fig. 5) and, for every k bits stored in said first latch circuit, said display data to bit lines of said memory in response to setting into said second operating mode (col. 14, lines 1-9).

42. Regarding claim 14, Nakano et al. further discloses a segment driver for forming a drive signal to be supplied to a segment line of said liquid crystal panel in response to read data from said memory. Col. 10, lines 17-19; Fig. 7, element 151.

43. Regarding claim 15, Nakano et al. further discloses a gradation voltage generator (col. 4, line 65 to col. 5, line 2; Fig. 1, element 110) and a gradation voltage select circuit for selecting, in response to read data from said memory, a desired gradation voltage out of a plurality of gradation voltages generated by said gradation voltage generator (col. 10, line 17-19; Fig. 7, element 157).

44. Regarding claim 16, Nakano et al. further discloses a common driver for forming a drive signal for periodically driving a plurality of common lines of said liquid crystal panel. Col. 6, lines 20-63; Fig. 1.

45. Regarding claim 18, all the limitations of claim 11 are found therein, and applicant is referred to the rejection of claim 11, *supra*, for those portions of claim 18. In addition, Nakano et al. further discloses a memory for storing display data to be displayed on a liquid crystal panel capable of color displaying (col. 6, lines 22-29; Fig. 3); a gradation voltage generator (col. 4, line 65 to col. 5, line 2; Fig. 1, element 110); a gradation voltage select circuit for selecting, in response to read data from said memory, a desired gradation voltage out of a plurality of gradation voltages generated by said gradation voltage generator (col. 10, lines 17-19; Fig. 7, element 157); and a segment driver for forming a drive signal to be supplied to a segment line of said liquid crystal panel on the basis of said selected gradation voltage (col. 9, lines 53-65; Fig. 7, elements 157, 158a, 158b).

46. Regarding claim 19, Nakano et al. further discloses a common driver for forming a drive signal for periodically driving a plurality of common lines of said liquid crystal panel. Col. 6, lines 20-63; Fig. 1.

47. Regarding claim 21, all the limitations of claim 18 are found therein, and applicant is referred to the rejection of claim 18, *supra*, for those portions of claim 21. In addition, Kudo et al. further discloses a mobile electronic apparatus comprising a liquid crystal panel (Fig. 1, element 9) including a plurality of common electrodes, a plurality of segment electrodes, and a plurality of dots driving by the difference in potential between said plurality of common electrodes and said plurality of segment electrodes (col. 7, line 64 to col. 8, line 7), a data processing unit for generating display data to be displayed on said liquid crystal panel (col. 13, line 26 to col. 15, line 23), wherein said display control device includes a k-bit first external terminal to which display data to be stored in said memory are supplied from said data processing unit (col. 9, lines 7-30; Fig. 2, element 21).

48. Regarding claim 22, Nakano et al. further discloses a common driver for forming a drive signal for periodically driving a plurality of common lines of said liquid crystal panel. Col. 6, lines 20-63; Fig.1.

49. Regarding claim 24, Nakano et al. further discloses that the liquid crystal panel is capable of color displaying in which each picture element comprises three dots of red, green and blue. Col. 6, lines 22-29; Fig. 3.

50. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. and Kudo et al. as applied to claim 21 above, and further in view of Taylor.

51. Nakano et al. and Kudo et al. fail to disclose a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory, said transfer circuit being controlled on the basis of information set in said mask setting circuit.

52. Taylor discloses a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory (col. 5, lines 30-52; Fig. 1, elements, 124, 126, 106, 108, 114, 116, 118, and 120), said transfer circuit being controlled on the basis of information set in said mask setting circuit (col. 5, lines 30-52).

53. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakano et al. and Kudo et al., with Taylor because Nakano et al. and Kudo et al disclose liquid crystal display control apparatuses, and Taylor discloses a dual port memory, and it is known in the art that many liquid crystal display control apparatuses (such as the one disclosed in Kudo et al.) contain a memory.

54. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. and Kudo et al. as applied to claims 11-16 above, and further in view of Taylor.

55. Nakano et al. and Kudo et al. fail to disclose a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory, said transfer circuit being controlled on the basis of information set in said mask setting circuit.

56. Regarding claim 17, Taylor discloses a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory, said transfer circuit being controlled on the basis of information set in said mask setting circuit. Col. 5, lines 30-52; Fig. 1.

57. Regarding claim 20, Taylor discloses a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory, said transfer circuit being controlled on the basis of information set in said mask setting circuit. Col. 5, line 30-52; Fig. 1.

58. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nakano et al. and Kudo et al., with Taylor because Nakano et al. and Kudo et al disclose liquid crystal display control apparatuses, and Taylor discloses a dual port memory, and it is known in the art that many liquid crystal display control apparatuses (such as the one disclosed in Kudo et al.) contain a memory.

Allowable Subject Matter

59. Claims 10 and 12 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Conclusion

60. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Washio et al., U.S. Pat. No. 6,618,043 (disclosing an image display device and image display method)
- Kumagawa et al., U.S. Pat. No. 6,597,337 (disclosing a driving method, drive IC, and drive circuit for liquid crystal display)
- Kubota et al., U.S. Pat. No. 6,559,824 (disclosing a matrix type image display device)
- Kubota et al., U.S. Pat. No. 6,437,768 (disclosing a data signal line driving circuit and image display apparatus)

- Lee, U.S. Pat. No. 6,421,038 (disclosing an active matrix liquid crystal display)
- Stiens, U.S. Pat. No. 6,407,732 (disclosing low power drivers for liquid crystal display technologies)
- Furuhashi et al., U.S. Pat. No. 6,295,045 (disclosing a liquid crystal display control device)
- Nakano et al., U.S. Pat. No. 6,229,513 (disclosing a liquid crystal display apparatus having a display control unit for lowering a clock frequency at which pixel drivers are driven)
- Yuki, U.S. Pat. No. 5,905,483 (disclosing a display control apparatus)
- Nakamura et al., U.S. Pat. No. 5,754,152 (disclosing a drive method and drive unit for a liquid crystal display device reducing variation of an applied voltage dependent upon display patterns)
- Imamura et al., U.S. Pat. No. 5,742,271 (disclosing a matrix type display device, electronic system including the same, and method of driving such a display device)
- Ohi, U.S. Pat. No. 5,604,511 (disclosing an active matrix liquid crystal display apparatus)
- Miner et al., U.S. Pat. No. 4,874,164 (disclosing a personal computer apparatus for block transfer of bit-mapped image data)
- Sugiyama et al., KR 97014533 A (disclosing a liquid crystal display controller of a liquid crystal display driver)
- Takahama et al., JP 09222947 A (disclosing a digitizer tablet)

- Munetsugu et al., EP 402850 A (disclosing a dot matrix display with upper and lower tabs)
- Takeda, EP 319661 A2 (disclosing a source electrode driving circuit for a matrix type liquid crystal display apparatus)
- EP 318517 B (disclosing display generator circuitry for a personal computer system)
- Harper et al., WO 9100587 A1 (disclosing a video image controller for a low power computer)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Conrad J. DeWitte whose telephone number is (703) 305-8626. The examiner can normally be reached on Monday through Friday, 8 a.m. to 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

CJD

JOSEPH MANCUSO
PRIMARY EXAMINER